REMARKS

The Examiner's Office Action mailed on July 8, 2003, has been received and its contents carefully considered.

Claims 1, 3, 4 and 8 have been amended, and new claims 15-20 have been added herein. Claims 1, 3, 4 and 8 remain the independent claims.

In the Action, the Examiner rejected claims 1 and 3-14 under 35 USC 103 (a) as being unpatentable over *Chen* (U.S. Patent No. 6,077,724) in view of *Ishio et al.* (U.S. Patent No. 6,118,184), further in view of Kim et al. (Korean Abstract Publ. No. 2002024958), and further in view of Han et al. (Korean Abstract Publ. No. 2001036630) Claims 1, 3, 4 and 8 have been amended. It is respectfully submitted that the claims, as amended, are clearly patentable over the applied art combination.

Claims 1 and 8 have been amended herein to further clarify that according to the claimed invention, integrated semiconductor chips are mounted on a nonconductive interposer substrate (which permits different electrodes thereon to be electrically isolated from each other). The interposer substrate has a through-hole through which electrodes formed on one of the chips are exposed. This permits external terminals, which are to be electrically connected to the chips, to be freely provided at any locations on a surface of the interposer substrate that is opposite to a surface on which the chips are mounted, and further permits these connections to be made with wires shorter than in the prior art. See, for example Fig. 1, in which the electrode 24 on the chip 10 to be wired with short wires 20 through the through-hole 16 to the terminals 32 on the surface of the interposer substrate 14 opposite to the surface on which the chips 10 and 12 are mounted.

In addition, amended claims 3 and 4 are directed to embodiments in which at least one of the chips is smaller than the size of the through-hole, so that the entire smaller chip can be located in the through-hole, as shown, for example in Figs. 6-9. Therefore, the thickness of the obtained semiconductor chip package can be reduced as compared with the prior art.

In the Action, the Examiner points to Chen as disclosing a multi-chip semiconductor package and fabrication method where the multi-chip semiconductor package fabrication method mainly combines LOC and BGA techniques to overlap one

chip on another chip in an IC component package. According to the Examiner, one chip uses the leads of a lead frame as a connection interface for the circuit on the chip to the outside, while another chip uses solder balls as a connection interface for the circuit on the chip to the outside. Further, according to the Examiner, the two chips are supported in a lead frame without a substrate used in a conventional BGA package.

The Examiner acknowledges that Chen fails to disclose the required bonding structure, bond wiring structure and the bond wiring structure in the specified manner. However, the Examiner points to Ishio as disclosing a semiconductor device sealed with a sealing resin and including structure to balance sealing resin flow where the required bonding structure is disclose. Further, asserts the Examiner, Kim discloses stacked chip packages where the required bond wiring structures is disclosed, and Han discloses stacked chip packages where the required bond wiring in the specified matter is disclosed. The Examiner argues it would have been obvious to one having ordinary skill in the art at the time the invention was made to include the required bonding structure, bond wiring structure and the bond wiring structure in the specified manner in Chen as taught by Ishio, Kim and Han respectively in order to have stacked semiconductor chips with better manufacturability.

The applicants respectfully disagree with the Examiner's argument. The Chen reference, by the Examiner's own admission, fails to disclose or even suggest a nonconductive interposer substrate or its use as in the claimed invention. Instead, Chen discloses only the electrically conductive electrode 241. Ishio fails to cure this defect in Chen's disclosure. Ishio discloses (see Fig. 2) only a die pad 5 disposed between two chips 1a and 1b and surrounded by leads 6. The leads 6 of Ishio appear to correspond to the electrodes 241 of Chen. However, neither Chen's electrode 241 nor Ishio et al.'s die pad 5 correspond to the through-hole-containing nonconductive interposer substrate of the present claimed invention defined in the independent claims.

The Han reference appears to add nothing relevant to the teachings of Chen and Ishio. Like Chen and Ishio, Han totally fails to disclose an interposer substrate. The elements 20 and 24 shown in the figure in Han are identified as leads, rather than any sort of substrate. Further, the figure discloses that the stacked chip package 100 has a lower chip 30 and an upper chip 40 arranged so as to have each of their active surfaces facing in

the same direction, rather than in opposite directions, as each of the independent claims of the present invention require.

The Kim reference discloses a stacked chip package 40, shown in the figure, in which a first chip 32 and a second chip 42 are disposed within chip mounting holes 35 and 45 formed in a center portion of substrate 31. As best understood, the Examiner appears to be arguing that substrate 31 and chip mounting holes 35 and 45 correspond to the interposer and the through-hole, respectively, of the presently claimed invention. However, in the present invention, the first chip is not disposed within the interposer, even when the size of the first chip is smaller than the size of the through-hole (see, for example, figs. 7 of the application). In independent claims 1 and 8, the second chip is mounted with its active surface on the first surface of the interposer substrate, and the first chip is mounted with its reverse side fixed to the reverse side of the second chip. In independent claims 3 and 4, the first chip is mounted on the first surface of the interposer substrate such that the through hole is covered by the first chip, or the first chip is mounted on the adhesive sheet which is fixed to the first surface of the interposer substrate and covers the through hole. In any case, is clear that what is being claimed is a structure in which the first chip is on or above the surface of the interposer substrate, and not within it. Combining Kim with the other references, none of which suggest any form of interposer substrate, would not alter the basic teaching of Kim or yield the claimed invention.

Further, the structure of the present invention is easier and less costly to fabricate than Kim because the interposer substrate thinner and only has one sized hole, which can therefore be punched rather than machined.

For at least the foregoing reasons, is respectfully submitted that claims 1 and 3-14 patentably distinguish over the applied art references, whether considered individually or in combination. The rejection accordingly should be withdrawn.

New claims 15-20 recites additional features that are disclose in the present application (see, for example, figs. 1 and 6-9). These new claims distinguish over the applied references for at least the reason that independent from claims 1, 3, 4 and 8.

Based on the above, it is submitted that the application is in condition for allowance and notice of such, with allowed claims 1 and 3-20, is earnestly solicited.

Respectfully submitted,

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Date

Phillip G. Avruch - Reg. No. 46,076
RABIN & BERDO, P.C.
Telephone: 202-659-1915
Telefax: 202-659-1898
CUSTOMER NO. 23995

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